MULTIPLE OUTPUT TIMING AND TRIGGER GENERATOR[*][†]

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Abstract

In support of the development of a multiple stage pulse modulator at the Los Alamos National Laboratory, we have developed a first generation, multiple output timing and trigger generator. Exploiting Commercial Off The Shelf (COTS) Micro Controller Units (MCU's), the timing and trigger generator provides 32 independent outputs with a timing resolution of about 500 ns.

The timing and trigger generator system is comprised of two MCU boards and a single PC. One of the MCU boards performs the functions of the timing and signal generation (the timing controller) while the second MCU board accepts commands from the PC and provides the timing instructions to the timing controller. The PC provides the user interface for adjusting the on and off timing for each of the output signals. This system provides 32 output or timing signals which can be pre-programmed to be in an on or off state for each of 64 time steps. The width or duration of each of the 64 time steps is programmable from 2 μs to 2.5 ms with a minimum time resolution of 500 ns. The repetition rate of the programmed pulse train is only limited by the time duration of the programmed event.

This paper describes the design and function of the timing and trigger generator system and software including test results and measurements.

I. INTRODUCTION

Many laboratory and engineering applications require multiple triggers or timing signals referenced to some given event or time. Typical commercial trigger or timing generators provide only a few, usually 2 to 4, independently adjustable signal outputs, but some applications require many more signals.

In [1] and [2] is described a multiple module Marx-Modulator with the capability to have each module triggered independently. Development work on the Marx-Modulator at Los Alamos National Laboratory identified the need for a scalable, programmable, multiple output trigger and timing generator in order to trigger each separate
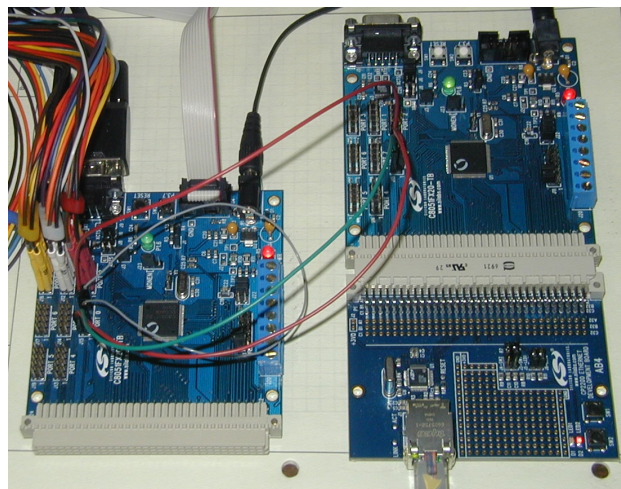
Figure 1. The two trigger generator MCU boards. The board on the right is the master controller and its ethernet adapter. The board on the left is the slave or timing controller.

module at a predetermined time. This capability allows one to "articulate" the high voltage output. Initially, only twelve separate timing signals were required for this diode-directed Marx-Modulator, however, eventually each of the 48 modules would require an independent trigger signal.

The first generation timing and trigger generator developed at Los Alamos allowed for only 32 separate outputs, however expansion to a higher number of outputs should be easily accomplished. In addition, each event is broken into 64 time steps. For each of the 64 time steps, each of the 32 outputs can be programmed to turn on, turn off, or maintain its current state. Based on the timing capabilities of the Microcontrollers used for this application, as well as the software controlling them, the time window for each event can range from 0 seconds to about 171 milliseconds.

This paper will provide details and descriptions of the hardware identified and implemented in the realization of the trigger generator, the system specifications, both prior to and post development, the performance of the first generation trigger generator, and some ideas for future direction.

II. HARDWARE AND SOFTWARE

A trigger generator system is comprised of two Silicon

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14. ABSTRACT
In support of the development of a multiple stage pulse modulator at the Los Alamos National Laboratory, we have developed a first generation, multiple output timing and trigger generator. Exploiting Commercial Off The Shelf (COTS) Micro Controller Units (MCUs), the timing and trigger generator provides 32 independent outputs with a timing resolution of about 500 ns. The timing and trigger generator system is comprised of two MCU boards and a single PC. One of the MCU boards performs the functions of the timing and signal generation (the timing controller) while the second MCU board accepts commands from the PC and provides the timing instructions to the timing controller. The PC provides the user interface for adjusting the on and off timing for each of the output signals. This system provides 32 output or timing signals which can be pre-programmed to be in an on or off state for each of 64 time steps. The width or duration of each of the 64 time steps is programmable from 2 s to 2.5 ms with a minimum time resolution of 500 ns. The repetition rate of the programmed pulse train is only limited by the time duration of the programmed event. This paper describes the design and function of the timing and trigger generator system and software including test results and measurements.

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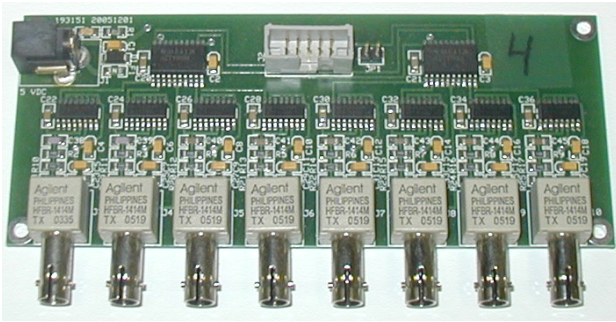
Figure 2. The 8 channel TTL signal to optical converter circuit.

Figure 3. The GUI from the PC based timing generation or editing software.

Laboratories C8051F120 embedded Microcontroller Unit (MCU) development boards along with one AB4 Ethernet adapter connected to one of the MCU boards [3].

The MCU board with the Ethernet adapter (called the master controller for purposes of this discussion) provides the link between a PC operated by a user and the second MCU board. The second MCU board (called the slave controller for purposes of this discussion) provides the requested timing signals by switching TTL voltage on and off at its I/O ports. Software running on the PC allows a user to develop the pulse timing specifications for an event. Communications between the PC and the first MCU board is accomplished using UDP datagrams over an Ethernet connection. Communications between the first and second MCU boards uses logic level serial or UART to UART communication at 115200 Baud. Figure 1 is a picture of the two MCU boards. The two boards are connected together with three wires for communication, and the timing board is connected to a logic analyzer. The Ethernet board and connection can be seen at the lower right.

The Silicon Laboratories C8051F120 was chosen for this application for several reasons. First, this MCU can achieve the fastest clock speed of any of the SiLabs MCU's at 100 MHz. Second, the C8051F120 provides the greatest number of I/O ports. This MCU provides 8 I/O ports with each port providing 8 pins for a total of 64 I/O lines or pins. Finally, this MCU provides 128 KB of flash memory which is important to this application because of of the implementation of a TCP/IP stack. In addition, the trigger generator makes use of some of the counter/timers, both of the UARTS, and the external memory interface, used in conjunction with the Ethernet adapter.

To convert the TTL signals to an actual trigger signal, a simple 8 channel TTL to optical converter circuit was fabricated. Figure 2 is a picture of one of the converter boards. At one side of the board is a standard ten pin header which accepts signals input from the timing and trigger MCU board, and at the other side of the board are the 8 fiber optic trigger outputs.

There are three separate programs or software applications required for the trigger generator system. Each MCU board runs separate software appropriate to its task. Both programs for the MCU boards were written in 'C' while the user interface, written to run on a PC, was written in 'C++'.
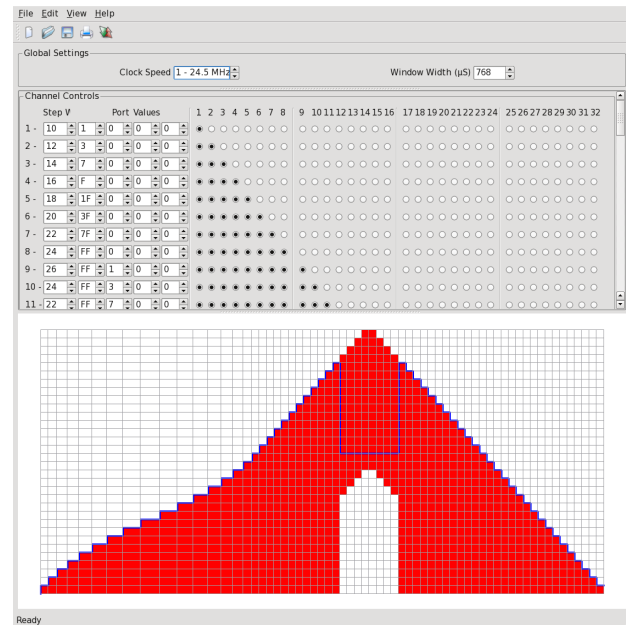
The MCU that controls the timing and produces the trigger signals (the slave controller) executes software that performs three basic functions. These functions are to check for commands from the master controller, monitor the soft and hard enable lines as well as the trigger input, and power on or off the appropriate I/O lines at the appropriate times.

The master controller executes software that implements a subset of a TCP/IP stack, waiting for UDP datagrams or packets sent from the PC containing timing specifications. Once new timing specifications have been received by the master controller, these data are passed on to the slave controller using two wire logic level serial communications.

Finally, software running on a PC (Linux OS, Windows OS, or Mac OS) allows the user to generate the timing for each of the 32 output channels at each of the 64 time steps, and transfer this data to the master controller. Figure 3 shows a screen clip of the PC software GUI. Note that the widths of each of the 64 time steps do not need to be the same, and in fact, can each be any value from the minimum time step to the maximum time step for any given clock speed, as shown in Table 1. Variable clock speeds are discussed in the following section.

III. SPECIFICATIONS

The original specifications for a multiple output trigger generator in support of the multiple module Marx generator called for at least 12 independently controlled timing signals with a time resolution of about 100 ns. The total time window or event length was specified to be on the order of 100's of microseconds to several 10's of milliseconds. Specifications concerning user interface and control were not initially defined.

One of the difficulties in the development of a system such as this timing and trigger generator is to obtain a time resolution of fractions of a microsecond over a period of time 4 to 5 orders of magnitude larger. The solution to this problem was to operate the timing board at different clock rates depending on the total time window or event length required. At the fastest MCU clock rate of 100 MHz, the time resolution is 500 ns, but the minimum time step length, because of software overhead, is 2 μs. Table 1 outlines the pulse generation specifications for the various clock speeds implemented on the trigger generator MCU board and controlled or switched by the software. Although the capabilities of the SiLabs C8051F120 MCU boards allow for many more clock speeds than are listed in Table 1, the clock speeds listed in the table are the only ones to have been implemented to date.
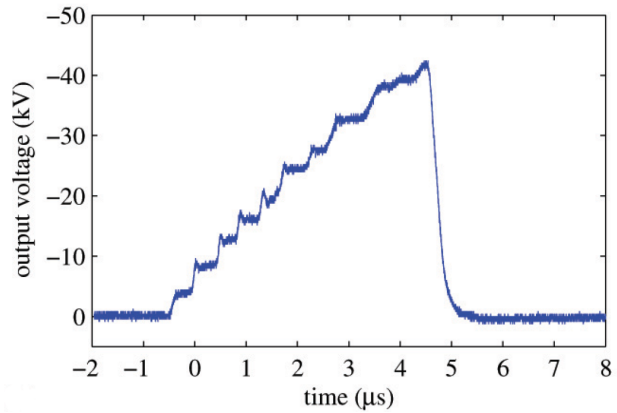
IV. PERFORMANCE

The timing and trigger generator has been tested both on the bench, with outputs monitored using a logic analyzer, and in the laboratory, with outputs driving a TTL to Optical converter, with the optical outputs triggering the Marx modules.

For this discussion the results from operation of the modular Marx modulator described in [1] and [2] will be presented. (Note that these data were collected before the minimum time step became introduced into the system.) This Marx modulator is a 48 stage device with a capability of up to 1.2 kV per stage. For this laboratory test, only twelve trigger outputs were used. Each output provided the trigger timing for four stages. Three different events or pulse

Figure 4. A saw tooth or ramp output voltage pulse from the modular Marx modulator with an initial charge voltage of 1.0 kV.
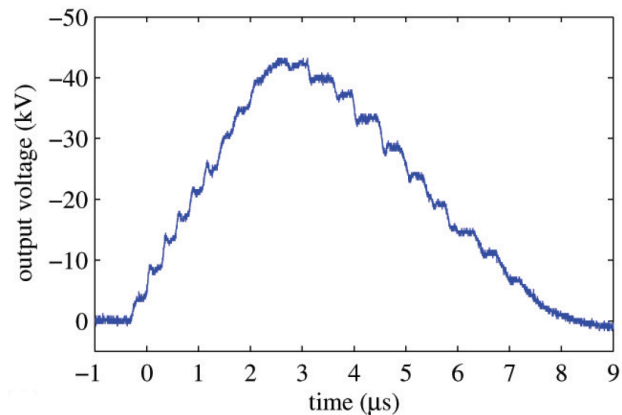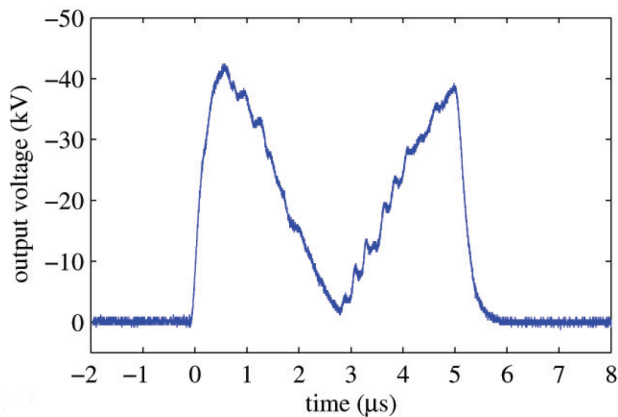

Figure 5. A triangle output voltage pulse from the modular Marx modulator with an initial charge voltage of 1.0 kV.

shapes were programmed into the MCU board to demonstrate both the capability of the Marx modulator to switch stages on and off at high voltage, and the ability of the trigger and timing system to provide control of the modulator. The results of this Marx modulator output articulation, with an initial charge voltage of 1.0 kV, is shown in the data presented in Figure 4, displaying a saw tooth or ramp waveform, Figure 5, displaying a triangle waveform, and Figure 6, displaying an inverted triangle waveform.

Clearly, the trigger and timing system performs the required function by providing the timing and trigger signals programmed by a user. Unfortunately, the timing resolution of 100 ns has not yet been realized. With the current system software overhead of about 2 μs some timing limitations exist.

V. FUTURE DIRECTIONS

There are several improvements that could be made to the

Table 1. Pulse generation specifications versus MCU board clock speed.

Clock Frequency	Min Time Step	Max Time Step	Instruction Cycle	Time Resolution
98.0 MHz	2.0 μs	655 μs	10.0 ns	500.0 ns
73.5 MHz	2.7 μs	891 μs	13.6 ns	680.0 ns
49.0 MHz	4.1 μs	1337 μs	20.4 ns	1020.0 ns
24.5 MHz	8.2 μs	2674 μs	40.8 ns	2040.0 ns

Figure 6. An inverted triangle output voltage pulse from the modular Marx modulator with an initial charge voltage of 1.0 kV.

trigger system described here, but by far the most important improvement would be to shorten or eliminate the current minimum time step limitation (2 μs at a 100 MHz clock speed). This limitation was introduced following reimplementation of the timing and control software for the slave MCU board. Also, with a clock speed of 100 MHz, a timing resolution of faster than 100 ns should be easily achievable. In addition, better error correcting algorithms implemented in all of the communications software would provide for a much more robust system. Finally, modification of the software would allow for the maximum number of output channels or signals for a single timing board. A SiLabs C8051F120 MCU board has 64 I/O signals, approximately 8 of which are dedicated to signals such as serial communications and enable or interlock signals, leaving about 56 I/O lines that could be used for timing and trigger signals in a single timing board implementation. The use of multiple timing boards would increase the number of I/O lines by about 56 per board.

VI. CONCLUSION

The first generation multiple output timing and trigger generator has provided a solution where no commercial off the shelf item has. Providing up to 32 channels of output and 64 time steps per event, the system is versatile enough to used for many applications. Although the timing and trigger generator was originally designed to provide a controller for a multiple module Marx generator, consideration and effort has been expended to make the system generic enough to be used for other applications.

VII. REFERENCES

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